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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
PORTKA, GARY J

ART UNIT	PAPER NUMBER
2188	29

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/748,589	Applicant(s) MARCH ET AL.	
	Examiner Gary J Portka	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *114-124* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *114-124* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 27 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 114-124 are pending.

2. Upon careful review, Examiner withdraws the previous acceptance of Applicant's intended narrow definition of the claim term "chip". However, since this definition was previously considered, both this definition as well as the broadest reasonable interpretation are considered in the art rejection below.

Information Disclosure Statement

3. The information disclosure submitted June 23, 2003 (paper no. 27) was considered.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 114, 116, 117, 119, 120, and 123 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leedy, U.S. Patent 6,208,545 B1 (hereinafter "Leedy"), in view of Shimoda et al., EP 1 017 100 A1 (hereinafter "Shimoda").

6. As to claims 114, 117, 120, and 123, Leedy discloses a modular three-dimensional electronic releasable memory device, system, and method comprising support element carrying ECC circuitry and memory, the memory comprising cells arranged in a plurality of layers stacked vertically above one another in a single device

(see Abstract, Figure 1a, 1c, and 2c, column 3 line 66 to column 4 line 22, and column 6 lines 61-67), with at least one data bit and one ECC bit (inherent for memory with ECC; note as cited below related description of how ECC works in conjunction with Barnett Figure 6). The modular housing protecting the circuits is met by the device shown in Figures 1a and 1c.

Leedy does not disclose that the device is fabricated on a single chip, instead that the three dimensional circuit is constructed by bonding multiple substrate layers using thermal diffusion metal bonding. However, the fabrication of a three dimensional device of multiple memory layers such as in Leedy on a single chip was well known in the art at the time of the invention. See Shimoda Abstract, Figure 21, and col. 6 lines 22-26 ("three-dimensional IC"). See also Shimoda column 36 line 55 to column 37 line 23, where it is taught that such three dimensional fabrication is relatively easy, increases device versatility, is highly reliable, and increases yield. The advantages of easy fabrication, versatility, reliability and high yield would have motivated an artisan to implement the three dimensional memory of Leedy on a single chip as taught by Shimoda. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to fabricate the memory layers on a single chip, because as taught by Shimoda this is relatively easy and increases versatility, reliability, and yield.

7. As to claims 116 and 119, the device of Leedy is selected from the recited group, since it is semiconductor-transistor-based.

8. Claims 115, 118, and 124 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leedy in view of Shimoda, and further in view of Zhang, U.S. Patent

5,835,396 (hereinafter "Zhang"); or over Leedy in view of Shimoda, and further in view of Johnson, U.S. Patent 6,034,882 (hereinafter "Johnson").

9. As to claims 115, 118, and 124, neither Leedy nor Shimoda disclose that the three-dimensional electronic device is a write-once device. However, Zhang teaches that a write-once memory device is advantageously implemented by a three-dimensional electronic device for improving density (see Abstract, column 1 lines 14-16 and 63-67, and column 2 lines 3-4 and 16-19); the motivation to implement a three-dimensional device as write-once clearly follows simply due to the desire to have well known write-once capability. Also, Johnson teaches similarly implementing a write-once device as a three-dimensional electronic device to increase the memory density (see Abstract, column 1 lines 14-60, and column 4 lines 11-22). Thus since the technology for implementing a write-once device as an electronic device was well known, and that a three-dimensional electronic device increases the memory density, an artisan would have been motivated to implement a three-dimensional device in Leedy in this manner. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a write-once device, because write-once electronic devices were well known design implementations of memory, and a three-dimensional device improves their memory density.

10. Claim 121 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leedy, in view of Shimoda, and further in view of Hayashi, U.S. Patent 5,708,667.

11. As to claim 121, Leedy does not disclose that the ECC generator is implemented in software. However, the implementation of ECC in software was well known in the art;

Hayashi describes an ECC implemented in software, as shown in Figure 1 and described at column 3 line 11 to column 4 line 13, and at column 7 lines 37-39. An artisan is well aware of the advantages of updatability and adaptability provided by an implementation in software, and these advantages would have motivated one to implement the ECC of Leedy in this manner. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the ECC in software, because this is well known and provides the system adaptability and updatability.

12. Claim 122 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leedy, in view of Shimoda, and further in view of Anderson, U.S. Patent 6,321,358 B1.

13. As to claim 122, Leedy does not disclose the ECC generator is part of the file system. However, it was well known to incorporate the ECC with the file system for a storage device, see Anderson Figure 31 and column 22 line 64 to column 23 line 10. An artisan would have recognized the advantage of compatibility with existing file systems implementing ECC to make the ECC generator part of the file system in the implementation of the device in Leedy. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the ECC generator as part of the file system, because this would make of the device of Leedy useable with known file systems which incorporate ECC generation.

14. Claims 114-120, and 123-124 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leedy in view of Zhang, or over Leedy in view of Johnson.

15. As to claims 114, 117, 120, and 123, Leedy discloses a modular three-dimensional electronic releasable memory device, system, and method comprising

support element carrying ECC circuitry and memory, the memory comprising cells arranged in a plurality of layers stacked vertically above one another in a single device (see Abstract, Figure 1a, 1c, and 2c, column 3 line 66 to column 4 line 22, and column 6 lines 61-67), with at least one data bit and one ECC bit (inherent for memory with ECC; note as cited below related description of how ECC works in conjunction with Barnett Figure 6). The modular housing protecting the circuits is met by the device shown in Figures 1a and 1c.

Leedy does not disclose that the device is fabricated on a single monolithic chip manufactured in situ (the previously accepted meaning of the term chip; see paragraph 2 above), instead that the three dimensional circuit is constructed by bonding multiple substrate layers using thermal diffusion metal bonding. However, the fabrication of a three dimensional device of multiple memory layers such as in Leedy on a single monolithic chip was well known in the art at the time of the invention. Zhang teaches that a memory device is advantageously implemented by a three-dimensional electronic device for improving density (see Abstract, col. 1 lines 14-16 and 63-67, col. 2 lines 1-9 and 16-26, and col. 10 line 49 to col. 11 line 28); the device of Zhang is taught to improve memory density, allow fast access, and may be manufactured using state-of-the-art semiconductor processing techniques, providing a multiple layer chip as recited. Also, Johnson teaches similarly implementing a memory device as a three-dimensional electronic device to increase the memory density (see Abstract, col. 1 lines 14-60, col. 4 lines 11-22, col. 12 line 42 to col. 13 line 25, col. 16 lines 4-20, and col. 18 lines 32-36). The device disclosed by Johnson is a multiple layer chip as recited, and an artisan

would have recognized that the advantages described with regard to Zhang above were provided by Johnson. The advantages of improved memory density, fast access, and ability to manufacture using state-of-the-art processing techniques would have motivated an artisan to implement the three dimensional memory of Leedy on a single monolithic chip as taught by Zhang or Johnson. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to fabricate the memory layers on a single monolithic chip, because as taught by Zhang and Johnson this is relatively easy and improves memory density, and allows fast access and state-of-the-art process manufacturing.

16. As to claims 115, 118, and 124, the teachings of Zhang and Johnson cited above both include a memory device that is write-once.

Double Patenting

17. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

18. Claims 114-120 and 123-124 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-31 of Tringali et

al., U.S. Patent No. 6,545,891 B1 in view of Leedy. The claims of Tringali disclose a modular memory device with support element, and three dimensional memory with plurality of layers stacked in a single chip. The claims do not disclose the ECC circuitry, however, as cited hereinabove Leedy teaches ECC circuitry as recited in an analogous three dimensional device. The ECC of Leedy provides the advantageous ability to correct errors, thus motivating an artisan to implement the claimed invention of Tringali with ECC circuitry as recited in the present invention.

Response to Arguments

19. Applicant's arguments filed July 2, 2003 have been fully considered but they are not persuasive.

Applicants have argued that the claim term "chip" means "a monolithic integrated circuit having all its components manufactured together in situ". Applicant has supported this argument with at length arguments and descriptions of how their manufacturing process differs from that of any of the cited references. Examiner responds, however, that this is not the broadest reasonable interpretation of the term "chip" commonly used in the art, see for example Shimoda which refers to the three dimensional device therein as an "IC", or integrated circuit, another term for chip (see Microsoft Press Computer Dictionary definition). Any further narrowing of the meaning is unjustifiably reading limitations from the specification into the claims. If Applicant intends the invention to include this limitation, it must be added to the claims.

Applicants have argued that Leedy teaches against using a single chip. Examiner does not agree; as previously stated Leedy more accurately teaches against

the use of planar (i.e., two dimensional) chips, in favor of three dimensional chips. Leedy proposes methods to improve upon the prior stacking of conventional 2D circuits to implement a 3D circuit. Examiner therefore maintains that an artisan familiar with the teachings of Leedy would have readily embraced the fabrication methods of Shimoda to achieve the advantages thereof.

Conclusion

20. Any inquiry concerning this communication from the examiner should be directed to Gary J. Portka at telephone number (703) 305-4033. The examiner can normally be reached on weekdays from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any response to this final action should be mailed to (or faxed as provided below):

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,
Arlington. VA., Fourth Floor (Receptionist).

The fax phone number for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final communications)

(703) 746-7239 (Official communications)

(703) 746-7240 (Status inquiries, draft communications)

Any inquiry of a general nature relating to this application or proceeding should be directed to the Group receptionist, whose telephone number is (703) 305-3900.

Gary J. Portka
Primary Examiner
July 31, 2003